In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-155. (Canceled)

156. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric membrane overlying the circuit devices.

157. (Currently Amended) The method of claim 156, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

158. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers ~~is~~ are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

159. (Previously Presented) The method of claim 158, wherein said stress is tensile.

160. (Previously Presented) The method of claim 157, comprising forming the at least one stress-controlled

dielectric layer by deposition of one or more stress-controlled dielectric films.

161. (Previously Presented) The method of claim 160, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

162. (Previously Presented) The method of claim 156, wherein the stress-controlled dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

163. (Previously Presented) The method of claim 162, wherein said stress is tensile.

164. (Previously Presented) The method of claim 156, wherein said substrate is a semiconductor wafer.

165. (Previously Presented) The method of claim 156, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

166. (Previously Presented) The method of claim 165, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

167. (Previously Presented) The method of claim 156, further comprising removing a major portion of the substrate

throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

168. (Previously Presented) The method of claim 167, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

169. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a stress-controlled dielectric layer overlying the circuit devices.

170. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

171. (Previously Presented) The method of claim 170, wherein said stress is tensile.

172. (Previously Presented) The method of claim 169, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

173. (Previously Presented) The method of claim 172, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

174. (Previously Presented) The method of claim 169, wherein said substrate is a semiconductor wafer.

175. (Previously Presented) The method of claim 169, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

176. (Previously Presented) The method of claim 175, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

177. (Previously Presented) The method of claim 169, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

178. (Previously Presented) The method of claim 177, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

179. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface; and

forming circuitry on the principal surface of the substrate with a stress-controlled dielectric layer.

180. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

181. (Previously Presented) The method of claim 180, wherein said stress is tensile.

182. (Previously Presented) The method of claim 179, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

183. (Previously Presented) The method of claim 182, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

184. (Previously Presented) The method of claim 179, wherein said substrate is a semiconductor wafer.

185. (Previously Presented) The method of claim 179, wherein the integrated circuit is able to have a major portion

of the substrate removed throughout a full extent thereof while retaining its structural integrity.

186. (Previously Presented) The method of claim 185, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

187. (Currently Amended) The method of claim ~~24~~ 179, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

188. (Previously Presented) The method of claim 187, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

189. (Previously Presented) A method of using an integrated circuit having a stress-controlled dielectric layer and interconnections formed passing through the stress-controlled dielectric layer, the method comprising:

transferring information through the interconnections formed passing through the stress-controlled dielectric layer.

190. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

191. (Previously Presented) The method of claim 190, wherein said stress is tensile.

192. (Previously Presented) The method of claim 189, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

193. (Previously Presented) The method of claim 192, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

194. (Previously Presented) The method of claim 189, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

195. (Previously Presented) The method of claim 194, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

196. (Previously Presented) The method of claim 189, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

197. (Previously Presented) The method of claim 196, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

198. (Currently Amended) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, interconnect circuitry interconnecting the data source and the data sink, the interconnections formed within ~~one or more~~ a stress-controlled dielectric ~~layers~~ layer, the method comprising:

transferring a plurality of data bytes between the data source and data sink of the interconnect circuitry of the integrated circuit.

199. (Currently Amended) The method of claim 198, wherein the ~~one or more~~ stress-controlled dielectric ~~layers~~ layer are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

200. (Previously Presented) The method of claim 199, wherein said stress is tensile.

201. (Currently Amended) The method of claim 198, further comprising forming the ~~one or more~~ stress-controlled dielectric ~~layers~~ layer by deposition of one or more stress-controlled dielectric films.

202. (Previously Presented) The method of claim 201, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

203. (Previously Presented) The method of claim 198, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

204. (Previously Presented) The method of claim 203, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

205. (Previously Presented) The method of claim 198, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

206. (Previously Presented) The method of claim 205, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

207. (Previously Presented) The method of claim 156, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

208. (Previously Presented) The method of claim 156, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

209. (Previously Presented) The method of claim 179, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

210. (Previously Presented) The method of claim 179, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

211. (Previously Presented) The method of claim 189, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

212. (Previously Presented) The method of claim 189, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

213. (Previously Presented) The method of claim 198, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

214. (Previously Presented) The method of claim 198, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

215. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers ~~is~~ are caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

216. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

217. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

218. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

219. (Currently Amended) The method of claim ~~120~~ 198, wherein the ~~one or more~~ stress-controlled dielectric ~~layers~~ layer are caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

220. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric membrane overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

221. (Previously Presented) The method of claim 220, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

222. (Previously Presented) The method of claim 220, wherein said substrate is a semiconductor wafer.

223. (Previously Presented) The method of claim 220, further comprising removing a major portion of the substrate.

224. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed prior to forming said circuitry.

225. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed after forming said circuitry.

226. (Previously Presented) The method of claim 220, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

227. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

228. (Previously Presented) The method of claim 227, wherein said stress is tensile.

229. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

230. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed prior to forming said circuitry.

231. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed after forming said circuitry.

232. (Previously Presented) The method of claim 220, comprising forming the stress-controlled dielectric membrane by deposition of one or more stress-controlled dielectric films.

233. (Previously Presented) The method of claim 232, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

234. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming a stress-controlled dielectric layer overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

235. (Previously Presented) The method of claim 234, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

236. (Previously Presented) The method of claim 234, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

237. (Previously Presented) The method of claim 236, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

238. (Previously Presented) The method of claim 234, wherein said substrate is a semiconductor wafer.

239. (Previously Presented) The method of claim 234, further comprising removing a major portion of the substrate.

240. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed prior to forming said circuitry.

241. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed after forming said circuitry.

242. (Previously Presented) The method of claim 234, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

243. (Currently Amended) The method of claim 234, wherein the stress-controlled dielectric ~~membrane~~ layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

244. (Previously Presented) The method of claim 243, wherein said stress is tensile.

245. (Previously Presented) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices;

forming a stress-controlled dielectric layer overlying said active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

246. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

247. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

248. (Previously Presented) The method of claim 245, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

249. (Previously Presented) The method of claim 248, comprising depositing at least some of the stress-controlled dielectric films using multiple RF energy sources.

250. (Previously Presented) The method of claim 245, wherein said substrate is a semiconductor wafer.

251. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

252. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

253. (Previously Presented) The method of claim 245, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

254. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

255. (Previously Presented) The method of claim 254, wherein said stress is tensile.

256. (Previously Presented) The method of claim 220, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

257. (Previously Presented) The method of claim 220, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

258. (Previously Presented) The method of claim 234, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

259. (Previously Presented) The method of claim 234, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

260. (Previously Presented) The method of claim 245, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

261. (Previously Presented) The method of claim 245, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

262. (Currently Amended) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers ~~is~~ are caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

263. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

264. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

265. (New) The method of claim 169, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

266. (New) The method of claim 169, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

267. (New) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

268. (New) The method of claim 229, wherein the one or more stress-controlled dielectric layers are caused to be elastic.

269. (New) The method of claim 229, wherein the one or more stress-controlled dielectric layers are caused to be elastic and the one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

270. (New) The method of claim 229, wherein the one or more stress-controlled dielectric layers are caused to be elastic and the one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

271. (New) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic.

272. (New) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic and the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

273. (New) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be elastic and the at least one or more stress-controlled dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

274. (New) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be elastic.

275. (New) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be elastic and

the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less.

276. (New) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

277. (New) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be elastic.

278. (New) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less.

279. (New) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

280. (New) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be elastic.

281. (New) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

282. (New) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

283. (New) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be elastic.

284. (New) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

285. (New) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

286. (New) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be elastic.

287. (New) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

288. (New) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

289. (New) The method of claim 245, wherein the stress-controlled dielectric layer is caused to be elastic.

290. (New) The method of claim 245 wherein the stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

291. (New) The method of claim 245, wherein stress-controlled dielectric layer is caused to be elastic and the stress-controlled dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

292. (New) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming a low stress dielectric layer overlying the circuit devices.

293. (New) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

294. (New) The method of claim 293, wherein said stress is tensile.

295. (New) The method of claim 293, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

296. (New) The method of claim 295, comprising depositing at least some of the low stress dielectric films using multiple RF energy sources.

297. (New) The method of claim 292, wherein said substrate is a semiconductor wafer.

298. (New) The method of claim 292, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof.

299. (New) The method of claim 292, further comprising removing a major portion of the substrate throughout a full extent thereof.

300. (New) The method of claim 299, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

301. (New) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

302. (New) The method of claim 292, wherein the integrated circuit is caused to be elastic.

303. (New) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to be elastic.

304. (New) The method of claim 292, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused

to have a thickness of about 50 microns or less and the low stress dielectric layer is caused to be elastic.

305. (New) The method of claim 292, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

306. (New) The method of claim 292, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

307. (New) A method of fabricating circuitry comprising the steps of:

providing a substrate having a principal surface;

forming circuit devices on the principal surface;

forming a low stress dielectric layer overlying the circuit devices; and

forming interconnections on the low stress dielectric layer between the circuit devices.

308. (New) The method of claim 307, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

309. (New) The method of claim 308, wherein said stress is tensile.

310. (New) The method of claim 308, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

311. (New) The method of claim 310, comprising depositing at least some of low stress dielectric films using multiple RF energy sources.

312. (New) The method of claim 308, wherein said substrate is a semiconductor wafer.

313. (New) The method of claim 307, wherein the circuitry is able to be thinned to about 50 microns or less throughout a full extent thereof.

314. (New) The method of claim 307, further comprising removing a major portion of the substrate throughout a full extent thereof.

315. (New) The method of claim 314, wherein the circuitry is caused to have a thickness of about 50 microns or less.

316. (New) The method of claim 307, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the circuitry is caused to have a thickness of about 50 microns or less.

317. (New) The method of claim 307, wherein the at least one low stress dielectric layer is caused to be elastic.

318. (New) The method of claim 307, wherein the low stress dielectric layer is caused to be elastic and the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

319. (New) The method of claim 307, wherein the low stress dielectric layer is caused to be elastic and the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the circuitry is caused to have a thickness of about 50 microns or less.

320. (New) The method of claim 307, further comprising:

providing a second circuitry overlying the circuitry; and

providing an interconnect that connects portions of the circuitry of the second circuitry and the circuitry.

321. (New) The method of claim 307, further comprising:

providing a plurality of circuits overlying the circuitry; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of circuitry and the circuitry.

322. (New) A method of fabricating interconnect circuitry comprising the steps of:

providing a substrate having a principal surface;

forming a low stress dielectric layer overlying the principal surface; and

forming interconnections on the low stress dielectric layer.

323. (New) The method of claim 322, wherein the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

324. (New) The method of claim 323, wherein said stress is tensile.

325. (New) The method of claim 323, comprising forming the low stress dielectric layer by deposition of one or more low stress dielectric films.

326. (New) The method of claim 325, comprising depositing at least some of low stress dielectric films using multiple RF energy sources.

327. (New) The method of claim 322, wherein the low stress dielectric layer is caused to be elastic.

328. (New) The method of claim 322, wherein the low stress dielectric layer is caused to be elastic and the low stress dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

329. (New) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices on the principal surface; and

forming an elastic dielectric layer overlying the circuit devices.

330. (New) The method of claim 329, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

331. (New) The method of claim 330, wherein said stress is tensile.

332. (New) The method of claim 329, further comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

333. (New) The method of claim 332, comprising depositing at least some of the elastic dielectric films using multiple RF energy sources.

334. (New) The method of claim 329, wherein said substrate is a semiconductor wafer.

335. (New) The method of claim 329, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

336. (New) The method of claim 335, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

337. (New) The method of claim 329, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

338. (New) The method of claim 337, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

339. (New) The method of claim 329, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

340. (New) The method of claim 329, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

341. (New) The method of claim 329, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

342. (New) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices; and

forming an elastic dielectric layer overlying said active devices;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

343. (New) The method of claim 342, wherein the elastic dielectric membrane is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

344. (New) The method of claim 343, wherein said stress is tensile.

345. (New) The method of claim 342, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

346. (New) The method of claim 342, comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

347. (New) The method of claim 346, comprising depositing at least some of the elastic dielectric films using multiple RF energy sources.

348. (New) The method of claim 342, wherein said substrate is a semiconductor wafer.

349. (New) The method of claim 342, further comprising removing a major portion of the substrate.

350. (New) The method of claim 349, wherein the major portion of the substrate is removed prior to forming said circuitry.

351. (New) The method of claim 349, wherein the major portion of the substrate is removed after forming said circuitry.

352. (New) The method of claim 342, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

353. (New) The method of claim 342, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

354. (New) The method of claim 342, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

355. (New) The method of claim 342, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

356. (New) A method of making an integrated circuit comprising:

forming on a substrate circuitry having active devices;

forming an elastic dielectric layer overlying said active devices; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

357. (New) The method of claim 356, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

358. (New) The method of claim 357, wherein said stress is tensile.

359. (New) The method of claim 356, wherein the major portion of the substrate is removed prior to forming said circuitry.

360. (New) The method of claim 356, wherein the major portion of the substrate is removed after forming said circuitry.

361. (New) The method of claim 356, comprising forming the elastic dielectric layer by deposition of one or more elastic dielectric films.

362. (New) The method of claim 361, comprising depositing at least some of the elastic dielectric films using multiple RF energy sources.

363. (New) The method of claim 356, wherein said substrate is a semiconductor wafer.

364. (New) The method of claim 356, wherein the major portion of the substrate is removed prior to forming said circuitry.

365. (New) The method of claim 356, wherein the major portion of the substrate is removed after forming said circuitry.

366. (New) The method of claim 356, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

367. (New) The method of claim 356, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

368. (New) The method of claim 356, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

369. (New) The method of claim 356, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

370. (New) A method of using an integrated circuit having an elastic dielectric layer and interconnections formed passing through the elastic dielectric layer, the method comprising:

transferring information through the interconnections formed passing through the elastic dielectric layer.

371. (New) The method of claim 370, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less.

372. (New) The method of claim 371, wherein said stress is tensile.

373. (New) The method of claim 370, further comprising forming the elastic dielectric layer by deposition of one or more stress-controlled dielectric films.

374. (New) The method of claim 373, comprising depositing at least some of the elastic dielectric films using multiple RF energy sources.

375. (New) The method of claim 370, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

376. (New) The method of claim 375, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

377. (New) The method of claim 370, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

378. (New) The method of claim 377, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

379. (New) The method of claim 370, wherein the elastic dielectric layer is caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

380. (New) The method of claim 370, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

381. (New) The method of claim 370, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

382. (New) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of

the integrated circuit, interconnect circuitry interconnecting the data source and the data sink, the interconnections formed within an elastic dielectric layer, the method comprising:

transferring a plurality of data bytes between the data source and data sink of the interconnect circuitry of the integrated circuit.

383. (New) The method of claim 382, wherein the one elastic dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less.

384. (New) The method of claim 383, wherein said stress is tensile.

385. (New) The method of claim 382, further comprising forming the elastic dielectric layers by deposition of one or more stress-controlled dielectric films.

386. (New) The method of claim 385, comprising depositing at least some of the elastic dielectric films using multiple RF energy sources.

387. (New) The method of claim 382, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

388. (New) The method of claim 387, wherein the integrated circuit is able to be thinned to about 50 microns or

less throughout a full extent thereof while retaining its structural integrity.

389. (New) The method of claim 382, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

390. (New) The method of claim 389, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

391. (New) The method of claim 382, wherein the elastic dielectric layers are caused to have a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

392. (New) The method of claim 382, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

393. (New) The method of claim 382, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

394. (New) The method of claim 156, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

395. (New) The method of claim 169, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

396. (New) The method of claim 179, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry, the principal surface overlying the barrier layer.

397. (New) The method of claim 220, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

398. (New) The method of claim 234, further comprising: providing a principal surface on the substrate; and forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

399. (New) The method of claim 245, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

400. (New) The method of claim 292, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

401. (New) The method of claim 307, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

402. (New) The method of claim 329, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

403. (New) The method of claim 342, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

404. (New) The method of claim 356, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.